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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/557,746	11/21/2005	Satoshi Shibata	071971-0432	2300

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EXAMINER	
CRAWFORD, LATANYA N	

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2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/557,746	SHIBATA, SATOSHI	
	Examiner	Art Unit	
	LATANYA CRAWFORD	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *1-4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the correspondence filed on 3/28/2008.

Examiner acknowledges claims 1-4 are canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5 -8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Keys (US pub no. 2004/0235280 A1)** in view of **Li (US Patent 7,094,671 B2).**

Regarding claim 5, Keys et al. discloses forming an amorphous layer **202** in a region from a surface of a semiconductor region of a first conductivity type to a first depth**([0020], lines 2-4)**; by heat treating the amorphous layer at a prescribed temperature, restoring a crystal structure of the amorphous layer **202** in a region from the first depth **211** to a second depth **202** that is shallower than the first depth so that the amorphous layer shrinks to the second depth **([0020], lines 17-23;[0034], lines 3-14; [0035], lines 7-11)**; after the heat treating, forming a first impurity layer of a second conductivity type which has pn junction at a third depth that is shallower than the second depth by introducing ions into the heat treated amorphous layer **([0020], lines 8-16; [0028], lines 1-13; [0036], lines10-14)**; activating the first impurity layer **([0037], lines 1-6)** but fails to teach heat treating the amorphous layer at a prescribed temperature without implanting ions into the amorphous layer.

However, Li et al. teaches heat treating the amorphous layer **230** at a prescribed temperature without implanting ions into the amorphous layer **(column 9, lines 33-40)**. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method for manufacturing a semiconductor device of Keys et al. with heat treating the amorphous layer at a prescribed temperature without implanting ions into the amorphous layer taught by Li et al. since doing so would increase the mobility of holes and electrons in the channel region resulting in a transistor device with a faster response time and increased drive current.

Regarding claim 6, Keys et al. teaches wherein the third depth is in a range of 5 nm to 15 nm **[0031].**

Regarding claim 7, Li et al. discloses fails to explicitly teach wherein the prescribed temperature is in a range of 475°C to 600°C, and the activation of the first impurity layer is conducted in a temperature range of 500°C to 700°C. However, Li et al. teaches wherein the prescribed temperature is in a range of 750°C or less **(column 9, lines 33-35)**, and the activation of the first impurity layer is conducted in a temperature range of 938.3 °C **(column 11, lines 55-60)**. Since the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a *prima facie* case of obviousness exists. *In re Wertheim*, 541 F.2d 257,191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed Cir. 1990)

Regarding claim 8, Li et al. discloses wherein a pattern of a gate electrode **242** that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region **202 (column 10, lines 60-63)**.

4. **Claims 9 & 12** are rejected under 35 U.S.C 103 (a) as being unpatentable in view of **Yu (US Patent 6,521,502 B1)**.

Regarding claim 9, Yu et al discloses forming a gate electrode **30** on a semiconductor region **12** of a first conductivity type **(column 4, line 13)**; forming an amorphous layer **25** in a region from a surface of the semiconductor region **12** of the first conductivity type to a first depth **(fig. 2; column 5, lines 8-9 & lines 31-36)**; by heat treating the amorphous layer at a prescribed temperature, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth **(fig. 3; column 6, lines 46-48 & 58-59)**; forming a first impurity layer **20 & 22 (40&42)** of a second conductivity type **(column 4, lines 43-48 & 64-65)** which has a pn junction at a third depth that is shallower than the second depth by introducing ions into the heat treated amorphous layer **(column 4, lines 43-48)**; forming a second impurity layer **50 & 52** of a first conductivity type which has pn junction **50 & 52** at a level that is shallower than the first depth and deeper than the third depth by introducing ions into the heat treated amorphous layer **(fig. 4; column 6, lines 8-14)**; and activating the first impurity layer and the second impurity layer **(column 7, lines 1-6)** . While Yu et al. discloses the heat treating after introducing ions to produce the layers claimed, the heat treating the amorphous layer without implanting ions into the amorphous layer to restore a crystal structure was not disclosed. The selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930)

Regarding claim 12, Yu et al. discloses wherein a pattern of a gate electrode **30** that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region **12 (column 5, lines 23-29)**.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Yu (US Patent 6,521,502 B1)** in view of **Keys (US pub no. 2004/0235280 A1).**

Regarding claim 10, Yu et al. discloses all the claim limitations of claim 9 but fails to teach wherein the third depth is in a range of 5 nm to 15 nm.

However, Keys et al. teaches wherein the third depth is in a range of 5 nm to 15 nm **[0031].** It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method for manufacturing a semiconductor device of Yu et al. with the third depth is in a range of 5 nm to 15 nm taught by Keys et al. since doing so would produce shallow junction and avoid increase in leakage current.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Yu (US Patent 6,521,502 B1)** in view of **Li (US Patent 7,094,671 B2)**

Regarding claim 11, Yu et al. discloses all the claim limitations of claim 9 but fails to teach wherein the prescribed temperature is in a range of 475°C to 600°C, and the activation of the first impurity layer is conducted in a temperature range of 500°C to 700°C.

However, Li et al. teaches wherein the prescribed temperature is in a range of 750°C or less **(column 9, lines 33-35)**, and the activation of the first impurity layer is conducted in a temperature range of 938.3 °C **(column 11, lines 55-60)**. Since the

claimed ranges "overlap or lie inside ranges disclosed by the prior art" a *prima facie* case of obviousness exists. *In re Wertheim*, 541 F.2d 257,191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed Cir. 1990)

7. **Claims 13, 15, & 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Keys (US pub no. 2004/0235280 A1)** in view of **Li (US Patent 7,094,671 B2).**

Regarding claim 13, Keys et al. discloses forming a gate electrode **508** on a semiconductor region **502** of a first conductivity type **([0039], lines 6-7)**; forming an amorphous layer in a region from a surface of the semiconductor region to a first depth **([0040], lines 1-3 & 10-12)** ; forming an insulating sidewall **514 & 516** on a side surface of the gate electrode **508** while restoring a crystal structure **([0042], lines 14-16)** of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth**([0020], lines 17-23;[0034], lines 3-14; [0035], lines 7-11)**, the restoration of the crystal structure of the amorphous layer being caused by heat treatment of a prescribed temperature which is conducted during formation of the sidewall **([0042], lines 9-12 &14-16);** after the heat treating, forming a first impurity layer of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions **([0020], lines 8-16; [0028], lines 1-13; [0036], lines10-14**) on both sides of the gate electrode **508** in the heat treated amorphous layer **([0043], lines 1-4)**; activating the first impurity layer **([0037], lines 1-6)** but fails to teach heat treating the amorphous layer at a prescribed temperature without implanting ions into the amorphous layer.

However, Li et al. teaches heat treating the amorphous layer **230** at a prescribed temperature without implanting ions into the amorphous layer **(column 9, lines 33-40)**. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method for manufacturing a semiconductor device of Keys et al. with heat treating the amorphous layer at a prescribed temperature without implanting ions into the amorphous layer taught by Li et al. since doing so would increase the mobility of holes and electrons in the channel region resulting in a transistor device with a faster response time and increased drive current.

Regarding claim 15, Keys et al. teaches wherein the third depth is in a range of 5 nm to 15 nm **[0031].**

Regarding claim 16, Li et al. discloses fails to explicitly teach wherein the prescribed temperature is in a range of 475°C to 600°C, and the activation of the first impurity layer is conducted in a temperature range of 500°C to 700°C. However, Li et al. teaches wherein the prescribed temperature is in a range of 750°C or less **(column 9, lines 33-35)**, and the activation of the first impurity layer is conducted in a temperature range of 938.3 °C **(column 11, lines 55-60).** Since the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a *prima facie* case of obviousness exists. *In re Wertheim*, 541 F.2d 257,191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed Cir. 1990)

Regarding claim 17, Li et al. discloses wherein a pattern of a gate electrode **242** that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region **202 (column 10, lines 60-63)**.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Keys (US pub no. 2004/0235280 A1)** in view of **Li (US Patent 7,094,671 B2)** as applied to claim 13 and further in view of **Yu (US Patent 6,521,502 B1).**

Regarding claim 14, Keys et al. as modified by Li et al. discloses all the claim limitations of claim 13 but fails to teach after the step of forming the first impurity layer, forming a second impurity layer of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer, wherein the second impurity layer is simultaneously activated in the step of activating the first impurity layer.

However, Yu et al. teaches after the step of forming the first impurity layer **20 & 22 (40 & 42)**, forming a second impurity layer **50 & 52** of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer **(fig. 4; column 6, lines 8-14 & 16-18)**, wherein the second impurity layer is simultaneously activated in the step of activating the first impurity layer **(column 7, lines 1-6)**. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method for manufacturing a semiconductor device of Keys et al. & Li et al with after the step of forming the first impurity layer, forming a second impurity layer of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer, wherein the second impurity layer is simultaneously activated in the step of activating the first impurity layer taught by Yu et

al. since doing so would form steep junctions, which is desirable for transistors with small dimensions.

Response to Arguments

9. Applicant's arguments with respect to claims 5-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are cited for disclosing related limitations of the applicant's claimed and disclosed invention: **Zhu et al. (US Patent 7,247,547 B2)**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LATANYA CRAWFORD whose telephone number is (571)270-3208. The examiner can normally be reached on Monday-Friday 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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